ABSTRACT

The present invention allows data transmissions to cross from one clock domain to another, in one embodiment, the invention includes an idle removing block operating at a first clock speed to remove idle bits from received data packets, a buffer coupled to the idle removing block to receive the data packets from the idle removing block, the buffer generating an idle insertion control signal to the idle removing block to enable the removal of idle bits by the idle removing block, and an idle insertion block coupled to the buffer to receive data packets from the buffer and insert idle bits into the data packets, the idle insertion block receiving an idle insertion control signal from the buffer to enable the insertion of idle bits.